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Design simulation of latch type voltage sense amplifier in low power and high speed operation for SRAM application

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Abstract

For an accurate sense operation, all nodes in the sense amplifier must be driven or equilibrated, earlier to clocking, to known voltage. For lowest power, it is needed that there are no DC paths from VDD to ground except during switching times. Also for a good comparison, the sense amplifier shouldn't have a memory of previous sensing operations. So we design sense amplifier with Removing Sense Amplifier Memory. In this paper we have propose and simulate low Power and great performance voltage latch Sense Amplifier for CMOSSRAM using VLSI design Technology i.e. primarily the plan of sense amplifier is designed & simulated using DSCH3. Sense Amplifier analyzed using MICROWIND3 in 65nm technology. Our effort is to diminish power consumption and expand the performance of sense amplifier. The results of simulation display that the proposed voltage latch sense amplifier design has benefit as compare to the conventional & improved conventional latch-type sense amplifier, based on 1.0V/65 nm CMOS technology. Proposed scheme improves sensing delay and also reduces power consumption.

Keywords:
Sense amplifier,
Simulation,
MICROWIND&DSCH,
Low power,
Technology scaling.

1. Introduction

Sensing the data from a memory cell is to detect voltage variations in bit-line. When a memory cell is read, the data (a charge) from the cell is sited on the bit-line [1]. The voltage that is placed on bit-line is changes. So change in voltage of the bit line appearances like a capacitor and that simply one word line can go high at a time in memory array. The voltage movement on the bit line, ΔV_{bit}, may be very, e.g., 50 mV or less, and so determining if the voltage is moving upwards or downwards can be challenging. In addition, we would like our sense amplifier to drive the bit line to full, valid, logic levels (for speed reasons in some memories and to refresh the cell in a dynamic RAM, DRAM). Improvement in CMOS technology is continues to diminish power consumption and to reduce delay and also required to integrate more function in a small silicon area. In 2010-2013 Deep Nano scale technologies [2] includes 32nm and 22nm processes appear to improve power, size, speed and increased integration of CMOS circuits we must scale down CMOS technologies[3].As the length of channel is decreases, the transistor

performance advances and per switching event power reduces[4]. The bit-line conditioning circuitry [5] is used to pre-charge the bit-lines high before operation. A simple conditioner consists of a pair of PMOS transistors. Sense amplifiers are highly susceptible to differential noise that is present on the bit-lines because they detect small voltage differences. If bit-lines are not pre-charged with enough voltage, residual voltages on the lines from the prior read may cause pattern-dependent failure [5]. An equalizer transistor can be added in the bit-line conditioning circuits to reduce the required pre-charge time. For a good comparison, the sense amplifier shouldn't have a memory of previous sensing operations [1]. To remove the sense amplifier's memory, all nodes in the sense amplifier must be actively driven to a known voltage. To stop the current that flows in the latch, breaking the connection between VDD and ground is one of themethods. In this paper a latch type low power voltage sense amplifier with removing sense amplifier memory circuit is designed using DSCH3 design tool on the basis of low power conventional voltage latch sense amplifier [6]. Latches arereplicated as the storage part which is used in several memoryapplications. In digital applications the latches planned along with sense amplifier will be the most capable memory element [7].The propagation delay is calculated as- Propagation delay = Rise time + fall time.

2.Improved conventional sense amplifier

Latch-type topology of sense amplifiers achieves fast conclusionsas a result of strong positive feedback and their differential input permits a low offset. The latch-type SA is an active comparator. Latch-type CMOS sense amplifier is realized in voltage mode and also in current mode [8]. The voltage mode of sense amplifier is commonly use because of its good sensing speed and small power consumption. The VLSA [9] senses the voltage difference (ΔV_{BL}) between the voltage of two bit-lines (V_{BL}) and (V_{BLB}) and then amplifies the differential voltage tofull swimming output voltages (V_{OUT} and V_{OUTB}).

The improved conventional latch type sense amplifier [6] is shown in fig. 1. In this fig. transistors P1, P2, N1 and N2 creating the main body of sense amplifier. Transistor N3 is used to control state of sense amplifier that are turn on/off by sense enable (SEN) signal. BL and BLN are the input/output of SRAM. When we write BL and BLN act as input and when we read from memory BL and BLN act as output of SRAM. Transistor P3 and P4 conclude in pre-charge circuit, BL and BLN pre-charge to VDD through P3 and P4. The transistor P5 works as balancing transistor that balances the initial voltage of two bit-lines. Initial voltage of bit-lines should be same this prevent bad turning of sense amplifier during signal amplification. The voltage difference between two bit-lines BL and BLN is transferred to sense amplifier by switching through transistor P6 and P7 that act as switch. The switching of transistor P6 and P7 is driven by the signal SEN, this is also use to enable sense amplifier. P6 and P7 are works as switching PMOS to transfer voltage difference from bit-lines to sense amplifier. Enable signal SEN turns off P6 and P7 through two inverters INV1 and INV2, then the large bit-line capacitance [10] is separated from sense amplifier, so that in the interior of the amplifier, bit-line capacitance will have little impact on the speed of the circuit and power consumption is reduced outstandingly.

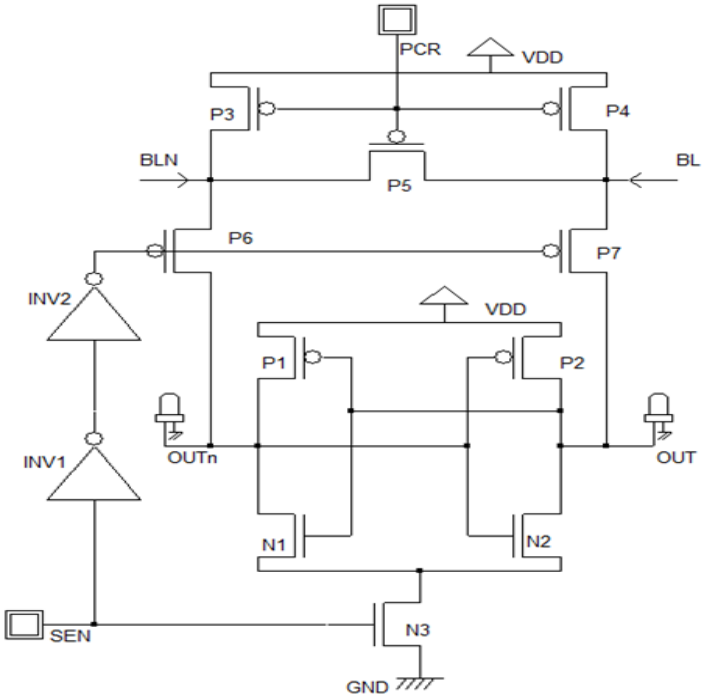

Fig. 1 Conventional voltage latch Sense Amplifier.

In sense amplifier that shown in fig.1 the voltage difference occurs at output due to change in device threshold of the transistor P6 and P7 so the output should be balance, for this we can adjust a balanced transistor between OUT and OUTn node.

3.Prior work

With the constant improvement of the technological level, the power supply voltage is designed to be lower, for example, the power supply voltage is as low as 1.0 V in 65 nm CMOS technology. On the basis of conventional sense amplifier the paper [6] described new latch type sense amplifier.

4.Proposed sense amplifier

In this paper, a different sense amplifier design is proposed on the basis of the improved conventional sense amplifiers the proposed design of voltage latch type sense amplifier is shown in fig. 2.
As shown in figure in the proposed design the transistors N3, N4, P11 and P12 are added for removing sense amplifier memory and also the transistor P10 is added to balance the output voltage. These transistors are controlled by SEN signal. In addition an inverter INV and transistors P13, P14 and N5 is added and controlled by PCR signal this mechanism used to control the switching of transistors P6 and P7. These transistors and inverter turn off transistors P6 and P7 until the bit-lines and sense amplifier are pre-charged to VDD, therefore this can prevent the bit-line current flowing to the sense amplifier to make the bit-line charge stored stably and then increase speed of the amplifier. Transistors P8 and P9 create cross coupling arrangement which can speed up the formation of bit-line voltage difference depending on positive feedback effect for the period of read operation. Transistors P3 and P4 makes the bit-line conditioning circuitry and transistor P5 work as an equalizer transistor.

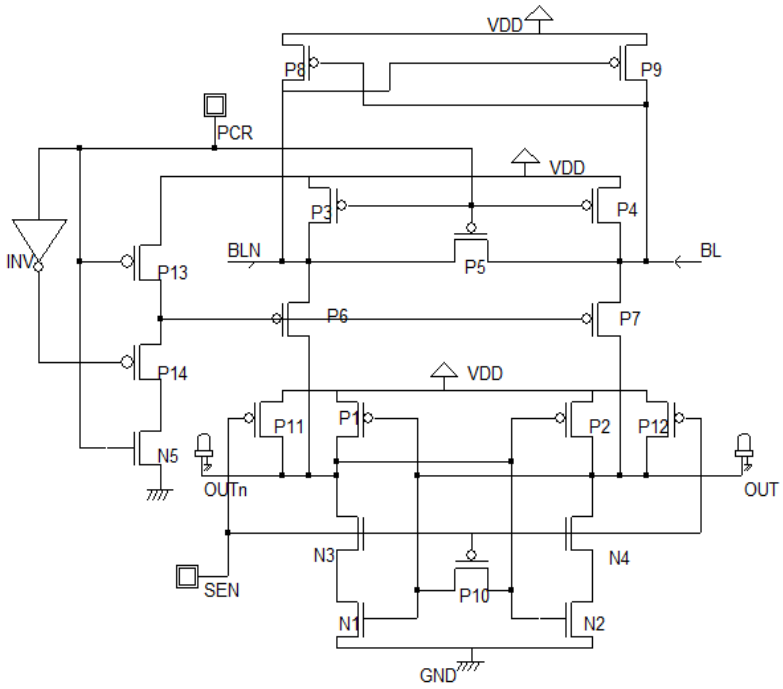

Fig.2 Proposed voltage latch type sense amplifier.

During read operation, When PRC is low the transistors P3 and P4 turn ON so the bit-lines are charged to VDD. At the same time the transistor P5 is also turn ON and balance the voltage on two bit-lines. Also until PRC is low transistors P6 and P7 are in OFF state this can prevent the bit-line current flowing to the sense amplifier. The low SEN signal turn ON transistors P11 and P12 and turn OFF transistors N3 and N4 so the voltage at output node is VDD and same time transistor P10 equalize the voltage between OUT and OUTn. When PRC and SEN signal goes high one of the bit-line goes down and latch is activated by turning ON transistors N3 and N4 and the bit-line voltage is amplified to its full logic level.

5. Simulation results

Simulations are performed using MICROWIND3 with 65 nm CMOS technology and also with 90 nm CMOS technology with 10ns scale. The simulation temperature is 27 ^{0}C and supply voltage is 1.0 V.The simulation is performed to compare the delay time and powerconsumption of the two sense amplifiers.
Simulation waveform of the conventional latch-type sense amplifier is shown in Fig. 3 and its delay time is 51 ps. And power consumption is 2.921 µW.

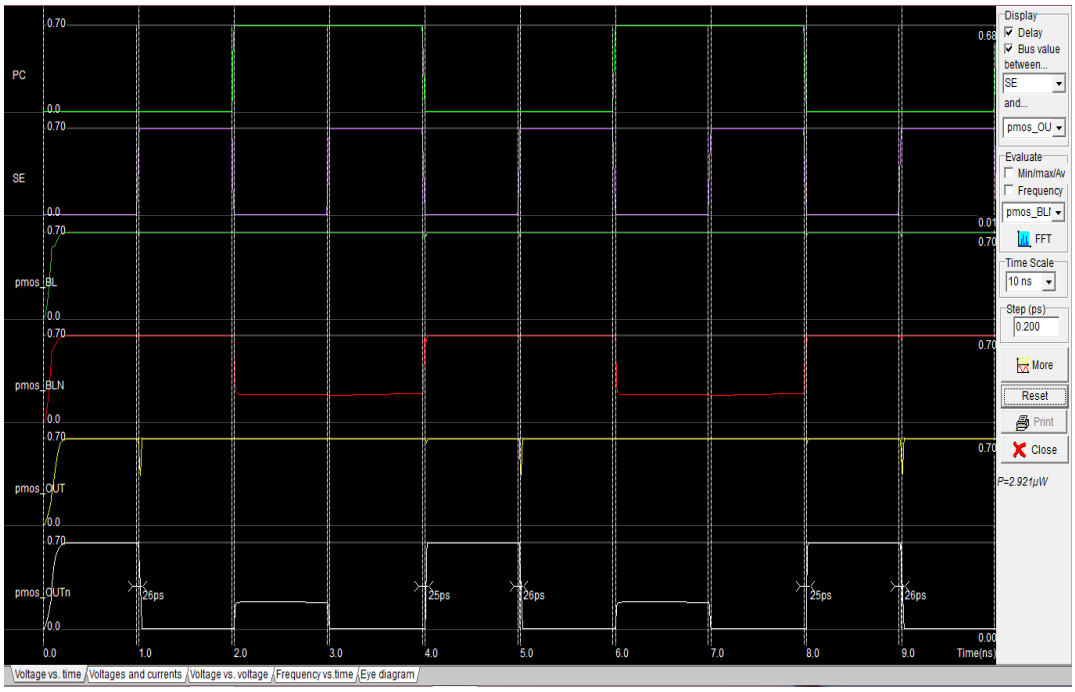

Fig. 3 Simulation waveform of conventional voltage latch Sense Amplifier.

Simulation waveform of the proposed sense amplifier is shown in Fig. 4. Delay time of this amplifier drops to 23 ps. And power consumption is 2.69 µW.

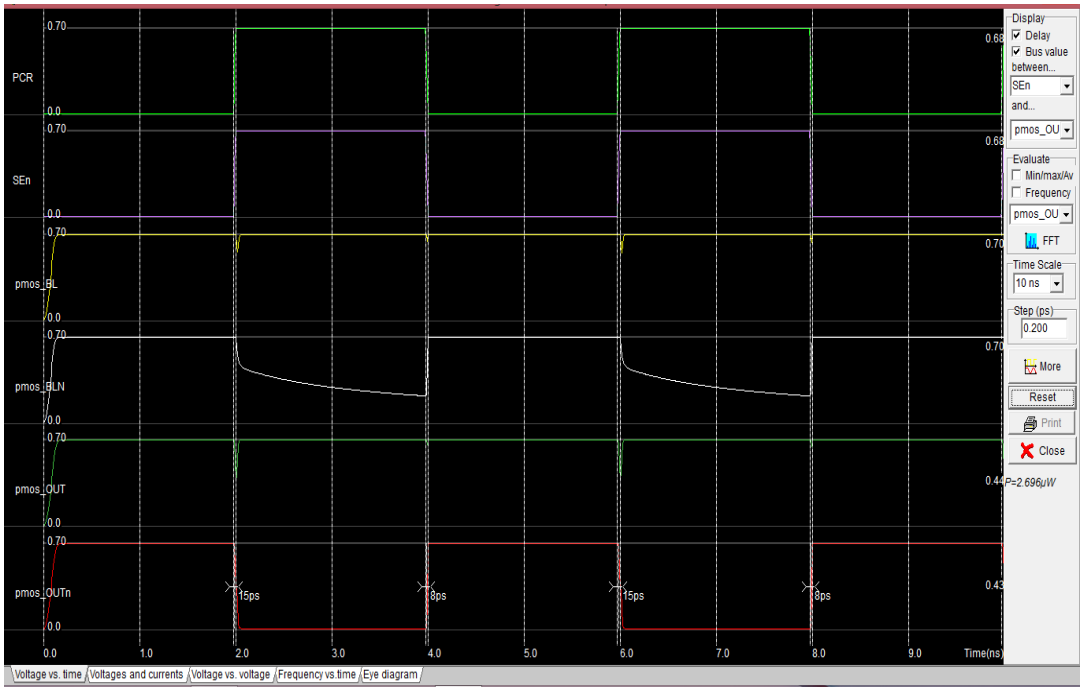

Fig. 4 Simulation waveform of proposed voltage latch Sense Amplifier.

We also simulate with 90nm technology. The simulation results are summarizing in Table 1&2.

Table-1 Simulation results of conventional voltage latch sense amplifier with different technologies.

Technology	Power (µW)	Delay (ps)
90nm	8.47	86
65nm	2.92	51

Table-2 Simulation results of proposed sense amplifier with different technologies.

Technology	Power (µW)	Delay (ps)
90nm	7.56	42
65nm	2.69	23

6. Parametric analysis

The parametric analysis between VDD v/s Power is performedin 65nm technology. The power dissipation at output node is analyzed. The results are shown in fig. 5&6.

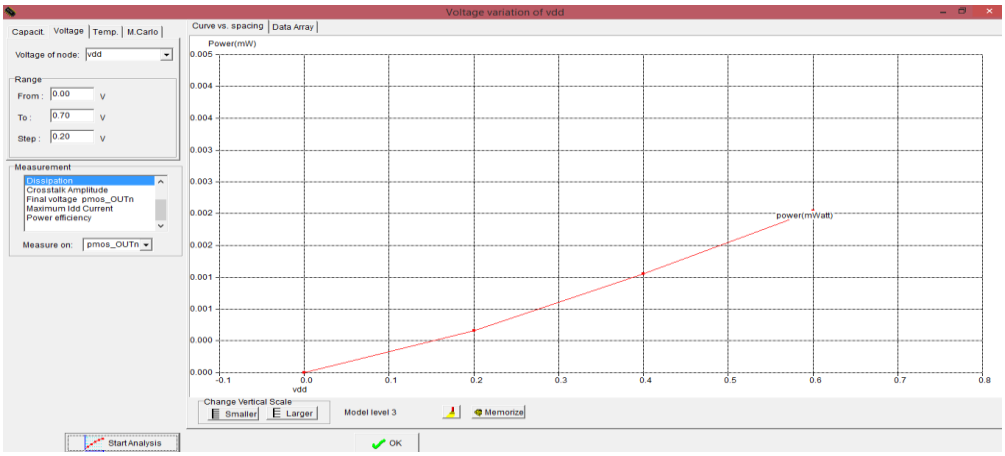

Fig. 5 Power analysis of reference sense amplifier

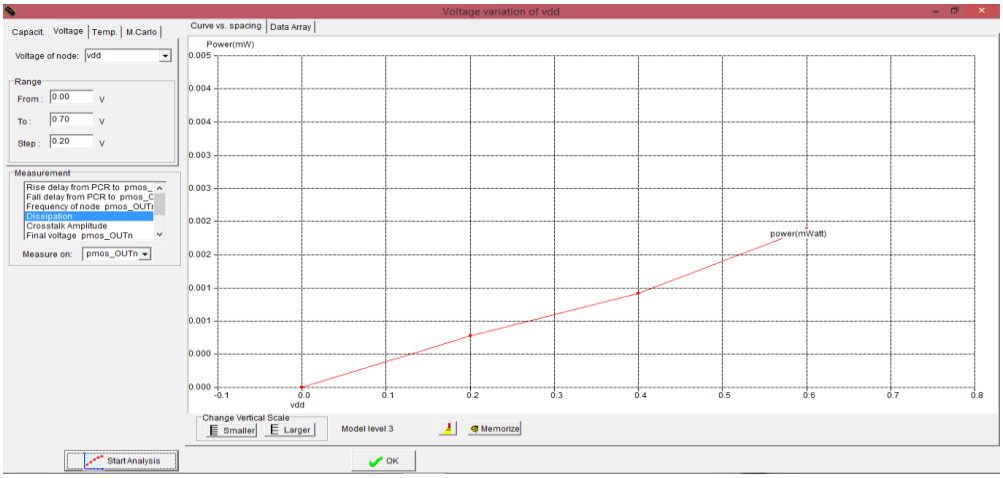

Fig. 6 Power analysis of proposed sense amplifier

7. Conclusion

This paper proposes a minimum delay sense amplifier appropriate for low voltage and low power application. Simulations are performed using MICROWIND3 for the 65nm and 90nm CMOS technology and the results show good performances of time delay and power consumption. In the power supply voltage of 1.0 V proposed sense amplifierreduces the delay to 23ps as conventional sense amplifier have delay 51ps and the average power consumption is also reduces to 2.69 µW. as conventional sense amplifier consume 2.921 µW.

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